

FIG. 1 is a perspective view of a parallel plate capacitor 100. The capacitor 100 includes an upper conductive layer 101, a dielectric layer 103, and a lower conductive layer 102. The upper conductive layer 101 and the lower conductive layer 102 are separated by the dielectric layer 103. The distance between the upper conductive layer 101 and the lower conductive layer 102 is denoted by 'd'. The area of the upper conductive layer 101 is denoted by 'A'.

100

UPPER CONDUCTIVE LAYER 101

DIELECTRIC  
LAYER 103

LOWER CONDUCTIVE  
LAYER 102

A

d

PARALLEL PLATE CAPACITOR

(PRIOR ART)

Fig. 1

FIG. 2 is a schematic diagram of a multi-layer printed circuit board (PCB) 200, showing a top layer 201, a middle layer 202, and a bottom layer 203. The top layer 201 includes a signal path 215<sub>1</sub> and a via 205<sub>1</sub>. The middle layer 202 includes a signal path 215<sub>2</sub> and a via 205<sub>2</sub>. The bottom layer 203 includes a signal path 215<sub>3</sub> and a via 205<sub>3</sub>. The vias 205<sub>1</sub>, 205<sub>2</sub>, and 205<sub>3</sub> are connected to a common signal path 215<sub>4</sub> which leads to a BICMC capacitor 210<sub>4</sub>. A BICMC capacitor 210<sub>1</sub> is also connected to the signal path 215<sub>2</sub>. An isolated area 213<sub>1</sub> is defined by a boundary 212<sub>1</sub> and 211<sub>1</sub>. A legend indicates that hatched areas represent Layer 1 Copper and solid black areas represent Layer 2 Anti-Copper.

200

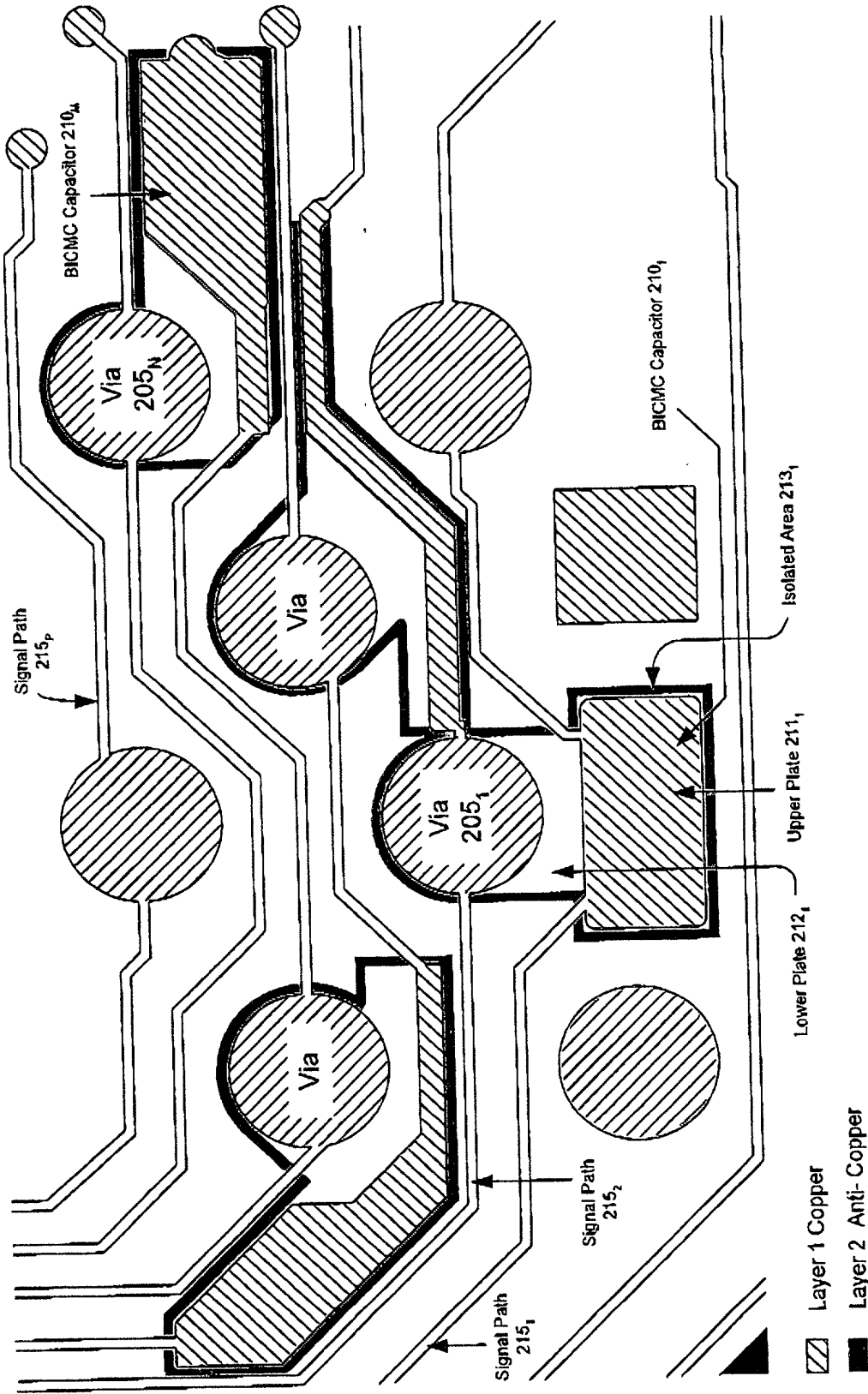


Fig. 2

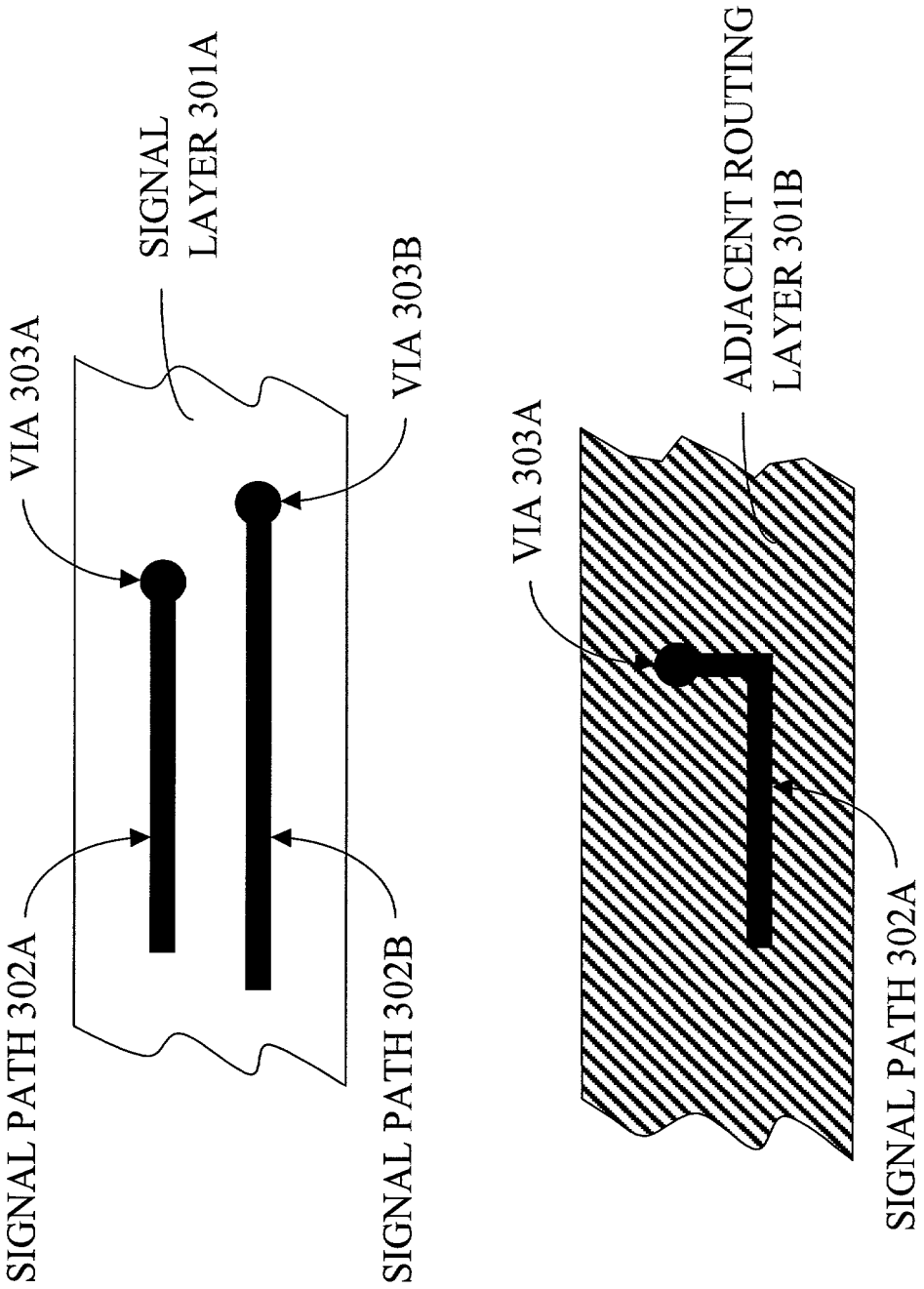


Fig. 3